Recommendations for Implementing a CNR Card using the Media Independent Interface (MII)

White Paper

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Contents

1. Overview

The Communication and Networking Riser (CNR) card provides a low cost solution for OEM manufactures with added flexibility for implementing audio, modem, local area network (LAN) interfaces, and broadband technologies (via USB). In addition to the flexibility and low cost, a CNR solution has significantly better noise immunity and signal quality due to the physical separation from the main board.

Currently, five interfaces are supported on CNR. The Media Independent Interface (MII) or the LAN Connect Interface (LCI) can be used for LAN, thus, allowing a maximum of four interfaces on a given CNR card. Refer to figure 1 shown below.

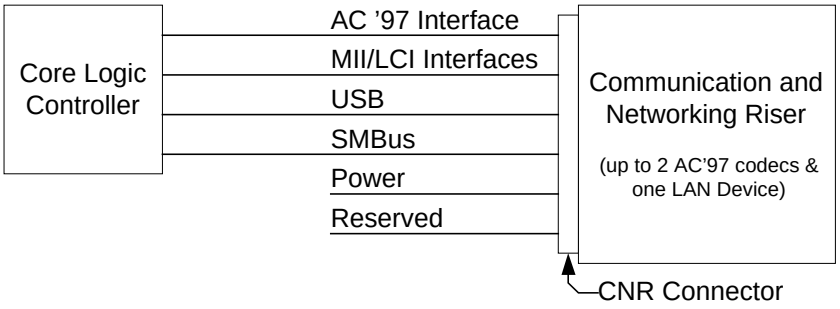

Figure 1 – Communication and Networking Riser card

A description of the interfaces are listed below:

- System Management Bus (SMBus) – Provides Plug and Play (PnP) functionality for the CNR card.
- AC '97 Interface – Supports audio and modem functions on the CNR card.
- LAN Connect Interface (LCI) – Provides LAN and Home Phone Networking Alliance (HPNA) capabilities for Intel® chipset based solutions (refer to the CNR specification).
- Media Independent Interface (MII) – Provides 10/100 switching and/or Home PNA for CNR platforms using the MII Interface.
- Universal Serial Bus (USB) – Supports devices implemented with a USB interface.

1.1 Purpose of this White Paper

Designers sometimes face issues implementing a CNR card into their motherboard design using the MII for LAN or HPNA. This white paper does not intend to be a design guide but instead recommends the configuration of the hardware and software required to interface a CNR card using the MII Interface. In addition, this paper will allow the designer to understand the basic requirements for implementing a CNR card into a motherboard design using the MII Interface for LAN.

2. Recommendations for Hardware Design and Configuration

A block diagram of the system interfaces and the CNR card is shown below.

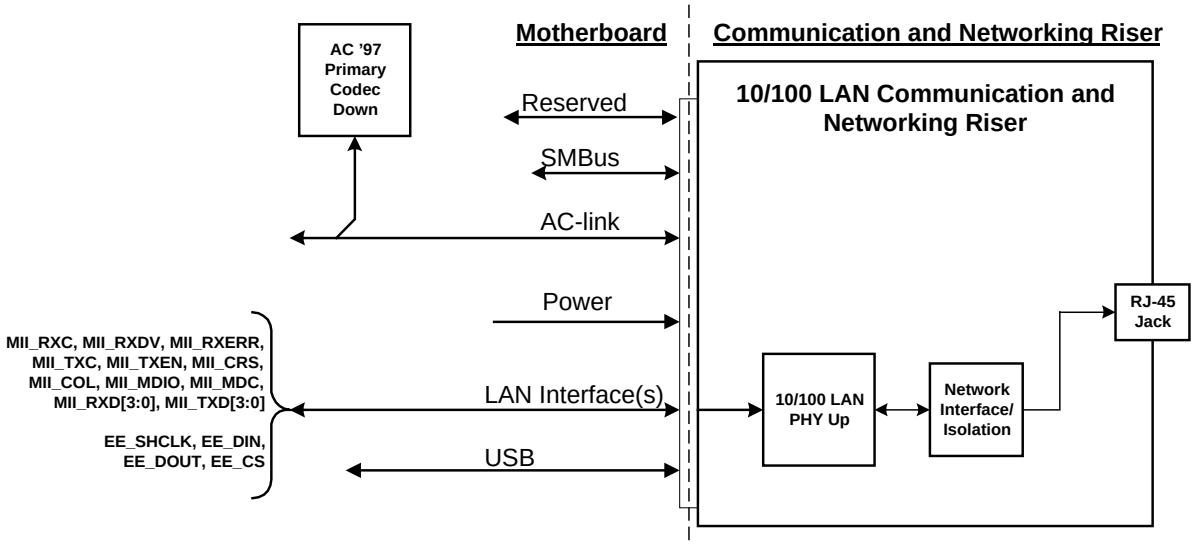

Figure 2 – 10/100 LAN on the CNR Card

Figure 2 shows a 10/100 LAN up on the CNR card and audio down on the main board. Notice that the MII Interface uses 17 pins connected between the motherboard and CNR card. The 17 MII pins interface directly to a Media Access Controller (MAC), which can be integrated or discrete on the motherboard. The four EEPROM signals (EE_SHCLK, EE_DIN, EE_DOUT, and EE_CS) wire directly to a LAN EEPROM, which contains the MAC address, as well as other MAC/PHY specific information. This implementation may be different from others. Refer to the vendor for recommendations.

2.1 Signal Descriptions and Connections

Tables 1 and 2, shown on the following pages, describe the signals required for interfacing a CNR card using the MII Interface with a Type-B connector on the main board.

Signal Name	Type	Pin Number	Signal Description
MII_TXD3	Input	B6	Bit 3 (MSB) of the 4-bit data bus transferring data from the MAC to the MII compliant PHY. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_TXD2	Input	A7	Bit 2 of the 4-bit data bus transferring data from the MAC to the MII compliant PHY. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_TXD1	Input	B8	Bit 1 of the 4-bit data bus transferring data from the MAC to the MII compliant PHY. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_TXD0	Input	A8	Bit 0 (LSB) of the 4-bit data bus transferring data from the MAC to the MII compliant PHY. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_TXC	Output	B3	Data clock from the MAC to the MII compliant PHY. For detailed information, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_TXEN	Input	B9	Transmit enable signal from the MAC to the MII compliant PHY. This signal indicates that the available on the MII_TXD[3:0] signals can be placed on the LAN wire. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_CRS	Output	A2	Carrier sense signal from the MII compliant PHY to the MAC. This signal indicates that there is traffic on the LAN wire. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_COL	Output	B2	Collision detect signal from the MII compliant PHY to the MAC. This signal indicates that a collision has occurred on the LAN wire. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_MDIO	In/Out	B1	Management data input/output signal between the Management Data Controller and the MII compliant PHY. This signal is used to carry bi-directional data for control and status registers. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_MDC	Input	A1	Management data clock signal from Management Data Controller to the MII compliant PHY. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.

Table 1 – CNR Connector Signals for the MII Interface

Signal Name	Type	Pin Number	Signal Description
MII_RXD3	Output	A12	Bit 3 (MSB) of the 4-bit data bus transferring data from the MII compliant PHY to the MAC. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_RXD2	Output	B11	Bit 2 of the 4-bit data bus transferring data from the MII compliant PHY to the MAC. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_RXD1	Output	A11	Bit 1 of the 4-bit data bus transferring data from the MII compliant PHY to the MAC. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_RXD0	Output	B12	Bit 0 (LSB) of the 4-bit data bus transferring data from the MII compliant PHY to the MAC. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_RXC	Output	A5	Data clock from a MII Interface compliant PHY to the MAC. For detailed information, refer to the current version MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_RXDV	Output	A4	Receive data valid signal from the MII compliant PHY to the MAC. This signal indicates that valid data is available on the MII_RXD[3:0] signals. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.
MII_RXERR	Output	B5	Receive error signal from the MII compliant PHY to the MAC. This signal indicates that an error has occurred during frame reception. For detailed information on this signal, refer to the current version of the MAC Specification and the IEEE 802.3u Specification. The reset state of this signal must meet the requirements set forth in the current version of the MAC Specification.

Table 1 (cont.) – CNR Connector Signals for the MII Interface

Table 2 shows three pins that are reserved signals for the Type-B connector.

Signal Name	Type	Pin Number	Signal Description
Reserved	N/A	A10	Reserved
Reserved	N/A	B14	Reserved
Reserved	N/A	A27	Reserved

Table 2 – CNR Reserved Signals for the B-Type Connector

2.2 Type-B Connector Pin Assignments

Figure 3, shown below, shows the pin-out for the Type-B connector using the MII Interface. The pin-out for a Type-B connector differs from a Type-A connector. Refer to the CNR Specification for complete specifications regarding the Type-A connector pin-out.

I/O Shield (back of system)

B1	MII_MDIO	MII_MDC	A1
B2	MII_COL	MII_CRS	A2
B3	MII_TXC	GND	A3
B4	GND	MII_RXDV	A4
B5	MII_RXERR	MII_RXC	A5
B6	MII_TXD3	GND	A6
B7	GND	MII_TXD2	A7
B8	MII_TXD1	MII_TXD0	A8
B9	MII_TXEN	GND	A9
B10	GND	RESERVED	A10
B11	MII_RXD2	MII_RXD1	A11
B12	MII_RXD0	MII_RXD3	A12
B13	GND	USB+	A13
B14	RESERVED	GND	A14
B15	+5Vdual	USB-	A15
B16	USB_OC#	+12V	A16
B17	GND	GND	A17
B18	-12V	+3.3Vdual	A18
B19	+3.3VD	+5VD	A19
	KEY	KEY	
B20	GND	GND	A20
B21	EE_DOUT	EE_DIN	A21
B22	EE_SHCLK	EE_CS	A22
B23	GND	SMB_A1	A23
B24	SMB_A0	SMB_A2	A24
B25	SMB_SCL	SMB_SDA	A25
B26	CDC_DN_ENAB#	AC97_RESET#	A26
B27	GND	RESERVED	A27
B28	AC97_SYNC	AC97_SDATA_IN1	A28
B29	AC97_SDATA_OUT	AC97_SDATA_IN0	A29
B30	AC97_BITCLK	GND	A30

Figure 3 – Type-B Connector Pin-Out using the MII Interface

Notice that signals B1 through B12 and A1 through A12 comprise the MII signals. The IEEE 802.3u Specification lists the TX_ERR as one of the signals used in the MII Interface. However, the CNR Specification does not support the TX_ERR signal. This is due to the fact that the TX_ERR signal is used only by LAN repeater devices. Since CNR is not intended for use as a repeater device, the TX_ER signal was not included on the CNR pin list for the MII Interface.

2.3 General Trace Routing and Considerations

LAN signals must be carefully routed to meet signal quality as mentioned in the CNR design guides. In addition, high-speed signals must be carefully routed to minimize cross talk and EMI. Listed below are some general guidelines for trace routing:

2.3.1 Crosstalk

Crosstalk causes degradation of signals and poor signal quality by affecting timing and functionality. Therefore, keep MII signals clear of high-speed signal traces including clock traces, oscillators, and other high frequency signals.

2.3.2 Trace Impedance Recommendations

It is highly recommended that proper trace impedance matching be maintained between the system board and the CNR card. A characteristic impedance of approximately 60 ohms is strongly recommended; otherwise, reflections can occur. Refer to the MAC/PHY manufacturer for their specific characteristic impedance requirements.

2.3.3 Trace Length

Keep trace lengths as short as possible as longer trace lengths are susceptible to changing rise and fall times, ringing, overshoot, undershoot, and propagation delays, which may lead to increased EMI and a reduction in the reliability of the MII Interface. The following general guidelines should be followed:

- High speed signals should be routed with minimal corners and sharp bends as this tends to increase the transmission line width, which can cause reflections and limit signal rise times.
- As a general rule of thumb, keep signal traces separated from the plane edges by a distance three times greater than the trace height above the ground plane to reduce coupling and signal interference.
- Keep traces and vias away from high harmonic devices (crystals, oscillators…. etc.) to prevent coupling and to ensure high signal quality.

2.3.4 Split Planes

It is crucial to route signals over a continuous plane without interruptions. Routing over a split plane will increase the inductance and EMI levels. Use stitching caps between the planes if necessary, but be advised that capacitors are frequency dependent and should only be used within a limited frequency band.

2.3.5 Signal Isolation

Follow these rules and considerations when routing signal traces:

- Separate and group signals by function on separate layers if possible.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize cross talk and to reduce the EMI from other signals.
- Avoid routing high-speed LAN traces near other high frequency signals such as video controller’s, cache controller’s, CPU’s, and other similar devices.

2.3.6 Stubs and Vias

Signal vias and stubs create EMI and signal quality problems. Keep them to a minimum and ensure adequate trace spacing. Keep vias as small as possible as larger vias have more inductance and capacitance, which can reduce the effectiveness of bypass capacitors in shorting the power planes at high frequencies.

2.4 Hardware Requirements

In order to ensure proper interoperability, there are a few hardware requirements on the CNR card as well as the motherboard.

2.4.1 CNR Card

The CNR card requires two EEPROM's that must be configured for the MII Interface: A Plug-and-Play (PnP) EEPROM and a LAN EEPROM. The PnP EEPROM stores information vital to the operating system and BIOS. Refer to the CNR specification for the device requirements and connectivity for the PnP EEPROM. The LAN EEPROM stores information pertinent to the LAN interface. See section 3.2 for further information regarding the LAN EEPROM.

2.4.1.1 PnP EEPROM

The PnP EEPROM has registers defined for LAN CNR Vendor ID and LAN CNR ID. The CNR PnP information will be provided to the operating system using a combination of an SMBus based EEPROM and specialized BIOS routines.

2.4.2 Motherboard

The designer must ensure a compatible and interoperable motherboard with the CNR card. A Type-B connector and a MAC must be incorporated into the motherboard design to assure proper compatibility.

2.4.2.1 Type-B Connector

A Type-B connector is required with the pinout shown in Figure 3 when implementing a CNR card using the MII Interface. Table 3, shown on the following page, shows different manufacturers' part numbers for connectors. These numbers tend to change; therefore, the designer should refer to the suppliers' part number and recommendations on the physical layout.

Manufacturer Name	Manufacturer's Part Number
Amp Incorporated	1-650090-2
Amp Incorporated	650090-6
Foxconn	EH03011-PL

Table 3 – Type-B Connector Manufacturers

Refer to the CNR specification for CNR Connector physical and dimensional requirements.

2.4.2.2 MAC

The motherboard designer must ensure proper compatibility between the MAC and the CNR card. Refer to the manufacture's voltage and current requirements to assure proper compatibility between the MAC and the CNR card.

2.5 Power Recommendations

Proper power considerations must meet the requirements of the CNR card. The designer must allow for enough power consumption by the CNR card. Refer to the appropriate data sheets and IEEE 802.3u specification for supply voltage and load current requirements for the MII Interface. The motherboard must supply the minimum current and voltage requirements and ensure that the CNR card does not exceed the power requirements specified in the CNR Specification to help ensure compatibility with the CNR card.

3. Recommendations for Software Design and Configuration

Software design and configuration consists of programming of the PnP EEPROM and the LAN EEPROM with the configuration of a LAN Interface Compliance Register.

3.1 CNR PnP EEPROM Configuration

The PnP EEPROM is configured using the CNR Test Suite (CNRTS) and supporting software as described in the CNR System Design and Developer's Guide obtained at: http://developer.intel.com/technology/cnr/.

The LAN Option Register contains individual bits that describe the required support of the LAN function implemented on the CNR board. Table 4 shows the LAN Option Register.

		Odd Byte Address (i.e. 01h)								Even Address (i.e. 00h)								
Register Address	Register Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
LP+000h	LAN Option Register	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	INTF	0000h
LP+002h	LAN CNR Vendor ID	LV15	LV14	LV13	LV12	LV11	LV10	LV9	LV8	LV7	LV6	LV5	LV4	LV3	LV2	LV1	LV0	0000h
LP+004h	LAN CNR Model ID	LM15	LM14	LM13	LM12	LM11	LM10	LM9	LM8	LM7	LM6	LM5	LM4	LM3	LM2	LM1	LM0	0000h
LP+006h	LAN Compliance	LC15	LC14	LC13	LC12	LC11	LC10	LC9	LC8	LC7	LC6	LC5	LC4	LC3	LC2	LC1	LC0	0000h

Table 4 – CNR EEPROM LAN Section Register Map

Bit 0 of the LAN Option Register, or the INTF register, must be set (1) to indicate that the LAN function implemented on the CNR card uses the MII interface. This can be accomplished by using the CNRTS. Figure 4, shown on the following page, shows the CNR Test Suite. Checking the LAN present box indicates that there is a MII compliant PHY or Platform LAN Connect (PLC) device available on the CNR card. The user must now enter the LAN Vendor ID, LAN Model ID, and check the MII Interface box.

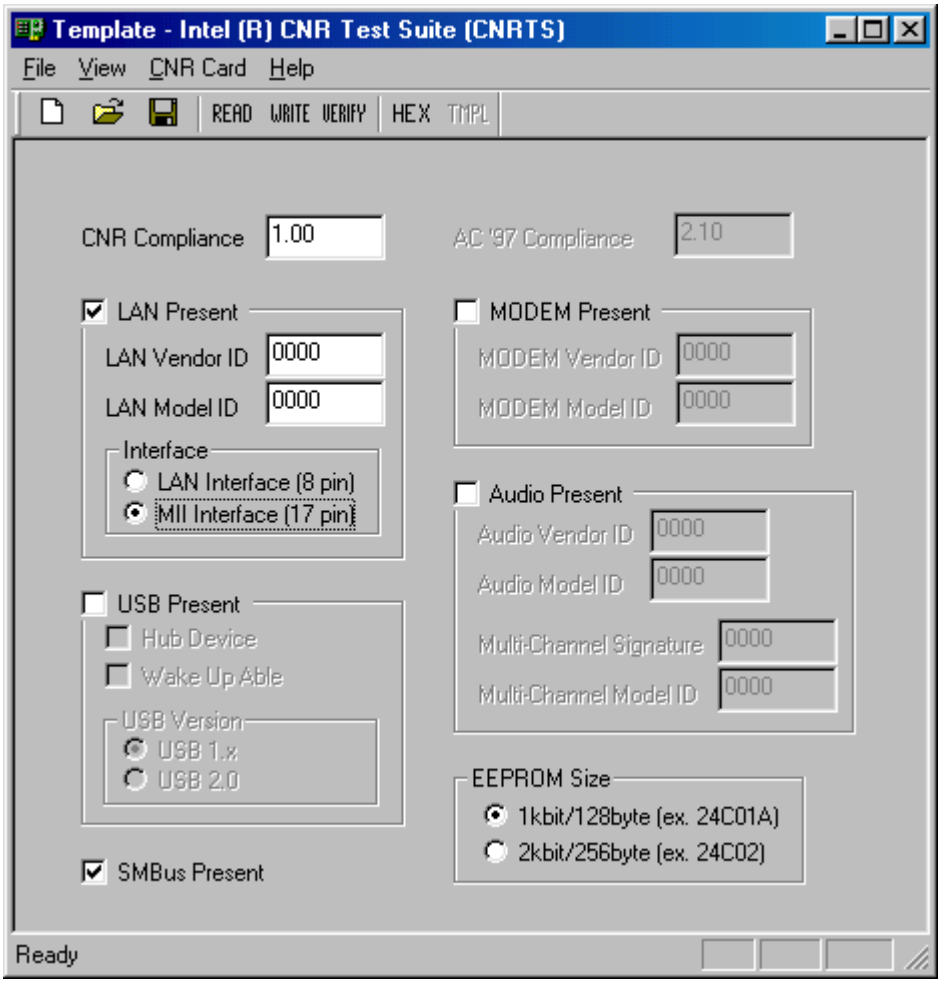

Figure 4 – CNR Test Suite Configuration using the MII Interface

The LAN Vendor ID, shown above, contains four hex digits that specify the manufacturer. This value is provided by the manufacturer of the CNR card and should match the corresponding value contained in the LAN EEPROM on the CNR card. The LAN Model ID contains four hex digits that specify the LAN model of the CNR card. The manufacturer of the CNR card also provides this value and should be identical to the corresponding value stored in the LAN EEPROM. The user must now write these values to the PnP EEPROM by clicking on the 'write' box located on the upper part of the CNR Test Suite.

3.2 LAN EEPROM

The LAN EEPROM contains PHY and MAC specific information. Usually, a LAN Vendor ID and a LAN Model ID are required and should be identical to those stored in the PnP EEPROM. The CNR specification provides a Microwire Interface for connecting the LAN EEPROM Interface of the CNR card to the MAC (note that the SMBus Interface can also be used, provided proper addressing is used). A table of the LAN Microwire EEPROM signals for the CNR card and descriptions are shown on Table 5.

Signal Name	Type	Pin Number	Signal Description
EE_SHCLK	Input	B22	This signal is the serial clock signal from the MAC Microwire* interface to the Microwire EEPROM (which stores MAC/PLC/PHY specific information) on the CNR board.
EE_DIN	Input	A21	This signal carries serial data from the MAC Microwire* interface to the Microwire EEPROM (which stores MAC/PLC/PHY specific information) on the CNR board. The EE_DIN signal on the CNR connector must be connected to the DIN pin on the Microwire EEPROM.
EE_DOUT	Output	B21	This signal carries serial data from the Microwire EEPROM (which stores MAC/PLC/PHY specific information) on the CNR board to the MAC Microwire* interface. The EE_DOUT signal on the CNR connector must be connected to the DOUT pin on the Microwire EEPROM.
EE_CS	Input	A22	The CNR board uses this signal to enable the serial EEPROM devices on the CNR board. When EE_CS is high (one) the Microwire EEPROM (for the LAN Interface) becomes active. When EE_CS is low (zero) the EEPROM is inactive. The resting state of this signal is low (zero). The state of this signal during reset must be low (zero).

Table 5 – CNR Connector Signals for the LAN Microwire EEPROM

Table 5 shows the LAN EEPROM signals using a LAN Microwire EEPROM. Programming implementations may vary from vendor to vendor. Refer to the vendor for configuration and programming guidelines. If implementing a LAN EEPROM on the SMBus, ensure that the PnP EEPROM address does not conflict with the LAN EEPROM address.

3.3 LAN Compliance Register Configuration

The LAN Compliance Register provides for a 16-bit value to identify the LAN Interface version that BIOS must be compliant with. This value is used to access and determine the functionality of the LAN components on the CNR board. The CNRTS version 1.0 does not support this. Therefore, the LAN Compliance Register should be properly configured by an experienced engineer to ensure proper compatibility with the CNR card and motherboard. Refer to the CNR Specification 1.1 for further information.

4. Summary

The designer must carefully integrate the MII Interface into their design to ensure proper interoperability. This white paper does not intend to be a design guide. Therefore, the designer should consult the appropriate data sheets and specifications for the requirements of the MII Interface and MAC as well as for the CNR card.

References

[1] Intel Corporation. *Communication and Networking Riser Specification 1.1*. http://developer.intel.com/technology/cnr/ (September 20, 2000).

[2] Intel Corporation. *Communication and Networking Riser Design Guide 1.0.* http://developer.intel.com/technology/cnr/ (September 20, 2000).

[3] Graham M, Johnson, H. *High Speed Digital Design: A Handbook of Black Magic*. New Jersey: Prentice Hall, 1993.

[4] IEEE 802.3u, Reconciliation Sublayer and Media Independent Interface (MII), in IEEE 802.3, 1995 edition.